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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,218	08/04/2003	Pantas Sutardja	MP0299	6850

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EXAMINER	
WANG, TED M	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/634,218	SUTARDJA ET AL.	
	Examiner	Art Unit	
	Ted M. Wang	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-97* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *See Continuation Sheet* is/are rejected.

7)☒ Claim(s) *6-9,12,15,18,19,21-25,37-40,45-47,55,57,59,60,62,63,65-70,78-81,84-86 and 93* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/04/2003.*11/28/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims rejected are 1-5,10,11,13,14,16,17,20,26-36,41-44,48-54,56,58,61,64,71-77,82,83,87-92 and 94-97.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

- Page 17, line 21, delete --- When ---.

Claim Objections

2. Claims 59, 69 and 70 are objected to because of the following informalities:

- In claim 59, line 3, change "first" to --- second ---.
- In claim 69, lines 1 and 3, delete --- third ---.
- In claim 70, line 1, change "first" to --- second ---.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 26, 28 and 72 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

- With regard claims 26, the limitation of "wherein said logic circuit comprises a second adder" as recited in claim 26 has not been taught in the specification. In

Fig.3 of the instant application, there in only one adder or combiner used in the logic circuit 220 to combine said data transfer control signal and said filtered clock information signal and provide an adjustment signal for said second periodic signal in response thereto.

- With regard claims 28 and 72, the limitation "an oscillator configured to provide a reference clock signal to said transmitter and said receiver." as recited has not been taught in the specification. The specification teaches only "Alternatively, phase detector 110 may receive a reference signal REF instead of data stream DATA. Reference signal REF may be a reference clock signal generated by an internal or external phase locked loop (PLL), crystal oscillator, or other source of a stable periodic signal (e.g., having a relatively constant frequency and/or amplitude)." as recited in paragraph 25. It teaches either receive DATA or REF oscillator by a phase detector but not both.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-5, 10, 11, 13, 27, 34, 51-54, 56, 58 and 71-75 are rejected under 35 U.S.C. 102(e) as being anticipated by Gregorius et al. (US 7,088,976).

- With regard claim 1, Gregorius et al. discloses an architecture for transferring data from a first device to a second device, comprising:

  a) a clock recovery loop (Fig.2 element 1, CDR) receiving said data (Fig.2 element RX) from said first device, said clock recovery loop providing a recovered clock signal (Fig.2 element 3 input);

  b) a filter circuit (Fig.2 elements 3, PLL, 16, MUX and 17, CSU) configured to filter information from said recovered clock signal (Fig.2 element 3, PLL, where PLL is used to attenuate jitter (column 2 lines 25-28) and contained a loop filter circuit as indicated in Fig.1 elements 5 and 19, column 5 lines 25-26 and column 7 lines 15-17) and provide a transmitter clock adjustment signal (Fig.2 element f_{CLK}) that adjusts said transmitter clock (Fig.2 element 17 output f_{TX}) in response to inputs from (i) said clock recovery loop (Fig.2 element f_{CLK}) and (ii) a transmitter clock circuit (Fig.2 element $f_{TXEXTLK}$); and

  c) a transmitter in communication with said filter circuit, configured to receive said transmitter clock adjustment signal and transmit said data to said second device in accordance with said transmitter clock signal (column 6 lines 12-31).

- With regard claim 2, Gregorius et al. further discloses a receiver (column 6 lines 12-31) in communication with said clock recovery loop and said filter circuit, configured to receive said data from a network (Column 4 lines 7-14, where the SONET stands for synchronous optical networking).

- With regard claim 3, Gregorius et al. further discloses wherein said clock recovery loop (Fig.1 and 2 element 1) comprises a first phase detector (Fig.1 element 4 and column 5 lines 24-25) configured to determine a phase difference between said recovered clock signal and either a reference clock signal or said data (column 5 lines 29-33).
- With regard claim 4, Gregorius et al. further discloses wherein said clock recovery loop further comprises a recovered clock adjustment circuit (Fig.1 elements 5 and 6 and column 5 lines 25-27, where the adjustment circuit is the charge pump, loop filter, and VCO) configured to adjust said recovered clock signal in response to said phase difference (column 5 lines 22-35).
- With regard claim 5, Gregorius et al. further discloses wherein said recovered clock adjustment circuit (Fig.1 elements 5 and 6 and column 5 lines 25-27, where the adjustment circuit is the charge pump, loop filter, and VCO) provides a recovered clock adjustment signal (Fig.1 elements 5 and 6 and column 5 lines 25-27, where the adjustment signal is from the charge pump and loop filter, 5, output to adjust the VCO in order to get the recovered clock) in response to said phase difference (column 5 lines 22-35).
- With regard claim 10, Gregorius et al. further discloses wherein said filter circuit comprises a jitter reduction circuit configured to reduce jitter in said input from said clock recovery loop and provide a filtered clock information signal in response thereto (column 2 lines 19-31).

- With regard claim 11, Gregorius et al. further discloses wherein said filter circuit further comprises a clock alignment block (Fig.2 elements 16 and 17) configured to (i) receive said recovered clock signal (Fig.2 element f_{CLK}) and said transmitter clock signal (Fig.2 element f_{TXEXT}) and (ii) provide a data transfer control signal (Fig.2 element f_{TX}) in response thereto.
- With regard claim 13, Gregorius et al. further discloses wherein said transmitter is configured to transmit serial data (column 4 lines 6-14, where Gregorius et al. teaches a transceiver to reconstruct the data which is transmitted over an optical transmission line, under SONET transmission standard, that is configured to transmit serial data.)
- With regard claim 27, which is a system claim related to claim 2, all limitation is contained in claim 2. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 34, Gregorius et al. further discloses a first port communicatively coupled to said receiver and a second port communicatively coupled to said transmitter, each of said first and second ports being configured to communicate with one or more external devices (column 1 lines 17-40 and column 4 lines 6-14).

  Gregorius et al. discloses a transceiver operated under SONET transmission standard. It is inherent that the transceiver has a first port communicatively coupled to said receiver (Fig.2 RX) and a second port

communicatively coupled to said transmitter, each of said first and second ports being configured to communicate with one or more external devices.

- With regard claim 51, which is a means plus function claim related to claim 1, all limitation is contained in claim 1. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 52, which is a means plus function claim related to claim 2, all limitation is contained in claim 2. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 53, which is a means plus function claim related to claim 3, all limitation is contained in claim 3. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 54, which is a means plus function claim related to claim 4, all limitation is contained in claim 4. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 56, which is a means plus function claim related to claim 10, all limitation is contained in claim 10. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 58, which is a means plus function claim related to claim 13, all limitation is contained in claim 13. The explanation of all the limitation is already addressed in the above paragraph.

- With regard claim 71, which is a mean plus function of system claim related to claim 27, all limitation is contained in claim 2. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 72, which is a mean plus function of system claim related to claim 28, all limitation is contained in claim 28. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 73, which is a mean plus function of system claim related to claim 30, all limitation is contained in claim 30. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 74, which is a mean plus function of system claim related to claim 32, all limitation is contained in claim 32. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 75 which is a system claim related to claim 34, all limitation is contained in claim 34. The explanation of all the limitation is already addressed in the above paragraph.

7. Claims 14, 16, 17, 20, 59, 61, 89-92 and 94-97 are rejected under 35 U.S.C. 102(e) as being anticipated by Sanduleanu (US 2003/0034849).

- With regard claim 14, Sanduleanu discloses a circuit for facilitating data transfer, comprising:

a) a clock alignment block (Fig.11 element LINEAR/BANG-BANG FD) configured to (i) receive first (Fig.11 element DATA) and second periodic signals (Fig.11 element COARSE/FINE matched VCO output (lower part)) and (ii)

provide a data transfer control signal in response thereto (Fig.11 element LPF2 output);

b) a first filter circuit (Fig.11 element FREQUENCY DETECTOR FD, CP1, LPF1 and LPF3) configured to receive first periodic signal information (Fig.11 element DATA) and provide a filtered clock information signal (Fig.11 element LPF3 output) in response thereto; and

c) a logic circuit (Fig.11 element COARSE/FINE matched VCO (lower part)) configured to combine said data transfer control signal (Fig.11 element LPF2 output) and said filtered clock information signal (Fig.11 element LPF3 output) and provide an adjustment signal for said second periodic signal in response thereto (Fig.11 element COARSE/FINE matched VCO (lower part)) output).

- With regard claim 16, Sanduleanu further discloses wherein said clock alignment block comprises a first phase detector (Fig.11 element LINEAR/BANG-BANG FD) configured to receive said first and second periodic signals.
- With regard claim 17, Sanduleanu further discloses wherein said clock alignment block further comprises a second filter circuit (Fig.11 element LPF2) configured to filter an output of said phase detector and provide said data transfer control signal.
- With regard claim 20, Sanduleanu further discloses wherein said first filter circuit comprises a frequency tracking loop (Fig.11 elements FREQUENCY

DETECTOR FD, CP1, LPF1 and Matched VCO, where FREQUENCY LOOP as indicated in Fig.11).

- With regard claim 59, which is a system claim related to claim 14, all limitation is contained in claim 14. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 61, which is a system claim related to claim 17, all limitation is contained in claim 17. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 64, which is a system claim related to claim 20, all limitation is contained in claim 20. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 89, which is a method claim related to claim 1, all limitation is contained in claim 1. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 90, Gregorius et al. further discloses receiving said data stream (Fig.11 element data) and recovering said first periodic signal therefrom (Fig.11 element LPF3 output).
- With regard claim 91, Gregorius et al. further discloses transferring data from said data stream to a transmitter configured to perform said transmitting step along a data path that does not include a first-in-first-out (FIFO) memory or an elastic buffer (Fig.11 where there is no first-in-first-out (FIFO) memory or an elastic buffer in the circuitry).

- With regard claim 92, which is a method claim related to claim 17, all limitation is contained in claim 17. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 94, Gregorius et al. further discloses the step of filtering said information from said first periodic signal (Fig.11 elements LPF1 and LPF3).
- With regard claim 95, Gregorius et al. further discloses wherein said information from said first periodic signal comprises recovered clock adjustment information (Fig.11 element LPF3 output).
- With regard claim 96, Gregorius et al. further discloses wherein said recovered clock adjustment information is configured to adjust a phase and/or frequency of said first periodic signal (Fig.11 element MATCHED VCO's, lower portion).
- With regard claim 97, Gregorius et al. further discloses wherein said recovered clock adjustment information is configured to adjust a phase of said first periodic signal (Fig.11 element Phase loop, where the phase loop includes linear/bang-bang FD, CP2, LPF2 and lower portion of matched VCO and paragraph 54).
- With regard claim 98 which is a method claim related to claim 20, I limitation is contained in claim 20. The explanation of all the limitation is already addressed in the above paragraph.

8. Claims 35, 36, 76 and 77 are rejected under 35 U.S.C. 102(e) as being anticipated by Hofmeister et al. (US 2004/0071389).

- With regard claim 35, Hofmeister et al. discloses a multiport device, comprising:

a) a plurality of receivers (Fig.1 element 108 in 102 and 120, transceiver, modules and Fig. 5A element 502), each coupled to a unique one of a plurality of clock recovery loops (Fig.5A element 510, CDR, where the network of the Fig.1 has plurality of transceiver 500),

b) a plurality of transmitters (Fig.1 element 112 in 102 and 120, transceiver modules, and Fig. 5A element 518), each coupled to a unique one of a plurality of filter circuits (Fig.5A element 514, RT) receiving recovered clock information from a corresponding one of the plurality of clock recover loops, and

c) a plurality of data paths (Fig.1 elements 124 and 126 and paragraph 009) for transferring data from one of the plurality of receivers to one of the plurality of transmitters.

- With regard claim 36, Hofmeister et al. further discloses a plurality of input ports (Fig.1 element 110 in 102 and 120, transceiver modules) communicatively coupled to the plurality of receivers (Fig.1 element 108 in 102 and 120, transceiver, modules and Fig. 5A element 502), and a plurality of output ports (Fig.1 element 114 in 102 and 120, transceiver modules) communicatively coupled to the plurality of transmitters (Fig.1 element 112 in 102 and 120, transceiver modules, and Fig. 5A element 518).
- With regard claim 76, which is a mean plus function of system claim related to claim 35, all limitation is contained in claim 35. The explanation of all the limitation is already addressed in the above paragraph.

- With regard claim 77, which is a mean plus function of system claim related to claim 36, all limitation is contained in claim 36. The explanation of all the limitation is already addressed in the above paragraph.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 29-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gregorius et al. (US 7,088,976) in view of Cai (US 7,050,777).

- With regard claim 29, Gregorius et al. discloses all of the subject matter as described in the above paragraph except for specifically teaching that the data transfer system could be implement in an integrated circuit.

  However, Cai teaches that the data transfer system could be implement in an integrated circuit (column 5, lines 50-65). One skilled in the art would have clearly recognized that the signal processing architecture of "Gregorius et al." would have been implemented in an integrated circuit. The implemented integrated circuit would perform same function of the discrete hardware for less expense, adaptability, and flexibility. Therefore, it would have been obvious to have using the single integrated circuit in "Gregorius et al." as taught by Cai in

order to reduce cost and improve the adaptability and flexibility of the communication system

- With regard claims 30 and 31, Gregorius et al. discloses all of the subject matter as described in the above paragraph except for specifically teaching wherein said receiver is further configured to have a deserializer to convert serial data from a network to parallel data for the transmitter.

However, Cai teaches wherein said receiver is further configured to have a deserializer (Fig.1 element 105) to convert serial data (Fig.1 element 102 and column 4 lines 36-39) from a network to parallel data (Fig.1 element 109 and column 5 lines 52-54) for the transmitter in order to convert the high speed input to multiple low speed output so that the cost of the communication system can be reduce to avoid the parallel same speed transceivers. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the deserializer as taught by Cai in which converting serial data from a network to parallel data for the transmitter, into Gregorius's transceiver so as to convert the high speed input to multiple low speed output so that the cost of the communication system can be reduce to avoid the parallel same speed transceivers.

- With regard claims 32 and 33, Gregorius et al. discloses all of the subject matter as described in the above paragraph except for specifically teaching wherein said transmitter is further configured to have a serializer to convert parallel data from the receiver to serial data for transmission to a destination.

However, Cai teaches wherein said transmitter is further configured to have a serializer (Fig.2 element 114 and column 6 lines 11-13) to convert parallel data (Fig.1 element 113 and column lines 5-9) from the receiver to serial data (Fig. 1 element 117 and column 6 lines 5-13) for transmission to a destination in order to convert the multiple low speed inputs to a high low speed output so that the cost of the communication system can be reduce to avoid the parallel same speed transceivers. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the deserializer as taught by Cai in which having a serializer to convert parallel data from the receiver to serial data for transmission to a destination, into Gregorius's transceiver so as to convert the high speed input to multiple low speed output so that the cost of the communication system can be reduce to avoid the parallel same speed transceivers.

11. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hofmeister et al. (US 2004/0071389) in view of Cai (US 7,050,777).

- With regard claim 41, Hofmeister et al. discloses all of the subject matter as described in the above paragraph except for specifically teaching that the multiport device could be implement in an integrated circuit.

However, Cai teaches that the multiport device could be implement in an integrated circuit (column 5, lines 50-65). One skilled in the art would have clearly recognized that the signal processing architecture of "Hofmeister et al." would have been implemented in an integrated circuit. The implemented

integrated circuit would perform same function of the discrete hardware for less expense, adaptability, and flexibility. Therefore, it would have been obvious to have using the single integrated circuit in "Hofmeister et al." as taught by Cai in order to reduce cost and improve the adaptability and flexibility of the communication system

12. Claims 42-44, 48-50, 82, 83, 87, 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saleh et al. (US 6,982,974) in view of Gregorius et al. (US 7,088,976).

- With regard claim 42, Saleh et al. discloses a network, comprising a plurality of systems (Fig.13 elements 1340, 1350 and 1360 matrix stages); and a plurality of communication devices (Fig.13 elements 1310(1, 1) – 1310(16, 16)), each of said communication devices being communicatively coupled to at least one of said systems.

  Saleh et al. further discloses a receiver (Fig.14 element 1428) communicatively coupled to said clock recovery loop (Fig.14 element 1430), configured to receive said data from a network (Fig.14 element 1413) and transfer said data to said transmitter (Fig.14 element 1443) and a clock recovery loop (Fig.14 element 1430) receiving said data from said first device (Fig.14 element 1413), said clock recovery loop providing a recovered clock signal (Fig.14 element 1430 output).

  Saleh et al. discloses all of the subject matter as described in the above paragraph except for specifically teaching b) a filter circuit configured to filter

information from said recovered clock signal and provide a transmitter clock adjustment signal that adjusts said transmitter in response to inputs from (i) said clock recovery loop and (ii) a transmitter clock circuit; and c) a transmitter in communication with said filter circuit, configured to receive said transmitter clock adjustment signal and transmit said data to said second device in accordance with said transmitter clock signal.

However, Gregorius et al. teaches b) a filter circuit (Fig.2 elements 3, PLL, 16, MUX and 17, CSU) configured to filter information from said recovered clock signal (Fig.2 element 3, PLL, where PLL is used to attenuate jitter (column 2 lines 25-28) and contained a loop filter circuit as indicated in Fig.1 elements 5 and 19, column 5 lines 25-26 and column 7 lines 15-17) and provide a transmitter clock adjustment signal (Fig.2 element f_{CLK}) that adjusts said transmitter clock (Fig.2 element 17 output f_{TX}) in response to inputs from (i) said clock recovery loop (Fig.2 element f_{CLK}) and (ii) a transmitter clock circuit (Fig.2 element $f_{TXEXTLK}$); and c) a transmitter in communication with said filter circuit, configured to receive said transmitter clock adjustment signal and transmit said data to said second device in accordance with said transmitter clock signal (column 6 lines 12-31).

It is desirable to have a transceiver circuit with a second PLL to filter out the jitter caused by the CDR (column 2 lines 19-31) and then using this filtered clock to regenerate transmitting clock f_{TX} in order to improve the communication quality. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include a transceiver circuit with a second

PLL to filter out the jitter caused by the CDR (column 2 lines 19-31) and then using this filtered clock to regenerate transmitting clock f_{TX} as taught by Gregorius et al. in order to improve the communication quality.

- With regard claim 43, Saleh et al. further discloses wherein said plurality of said systems are embodied on a single integrated circuit (column 14 lines 22-31).
- With regard claim 44, the modified circuit of the Saleh et al. and Gregorius et al. as addressed in claim 44, further teaches wherein said plurality of said systems receives serial data from said plurality of communications devices (column 7 lines 11-21).
- With regard claim 48, Saleh et al. further discloses a network controller or logic configured to select a first device of said plurality of communications devices from which serial data is to be transmitted (Fig.13 element 1330 and column 18 lines 36-65).
- With regard claim 49, Saleh et al. further discloses a network controller or logic configured to select a second device of said plurality of communications devices from which serial data is to be transmitted (Fig.13 element 1330 and column 18 lines 36-65).
- With regard claim 50, Saleh et al. further discloses wherein said network controller or logic is further configured to select a data path through said plurality of said systems to receive said serial data from said first device and transmit said serial data to said second device (Fig.13 element 1330 and column 18 lines 36-65).

- With regard claim 82, which is a mean plus function of system claim related to claim 42, all limitation is contained in claim 42. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 83, which is a mean plus function of system claim related to claim 44, all limitation is contained in claim 44. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 87, which is a mean plus function of system claim related to claim 48, all limitation is contained in claim 48. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 88, which is a mean plus function of system claim related to claim 50, all limitation is contained in claim 50. The explanation of all the limitation is already addressed in the above paragraph.

Allowable Subject Matter

13. Claims 6-9, 12, 15, 18, 19, 21-25, 37-40, 45-47, 55, 57, 60, 62, 63, 65-70, 78-81, 84-86 and 93 are objected to as being dependent upon an objected claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

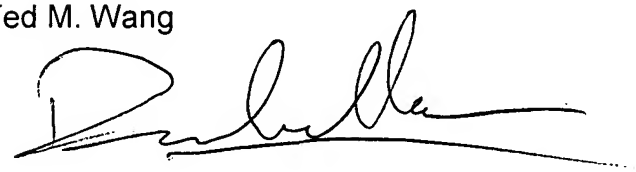
14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted M Wang
Examiner
Art Unit 2611

Ted M. Wang



DAC HA
PRIMARY EXAMINER